THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 10

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANK L. THIEL

Appeal No. 95-3798
Application 08/063,968[1]

ON BRIEF

Before THOMAS, LEE and TORCZON, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by prior art. No claim has been allowed.

Reference Relied on by the Examiner

Sakai	U.S. Patent No. 4,375,598	March 1, 1983

The Rejections on Appeal

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[1] Application for patent filed May 19, 1993.

Claims 1-16 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Sakai.

The appellant has stated (Br. at 5) that claims 1-7 stand or fall together and claims 8-16 stand or fall together.

The Invention

The invention is directed to a circuit which may be used as a comparator. It includes a differential input stage having a pair of transistors arranged in differential mode and a pair of transistors arranged in current mirror mode. It also includes a hysteresis stage which has a conductance path coupled in parallel to the conductance path of one of the current mirror transistors and which is responsive to the conductance state of one of the differential mode transistors for enabling current through the hysteresis stage.

Claims 1 and 8 are independent claims. All other claims are dependent claims. Claim 1 reads as follows:

> In combination:
>
> a first pair of transistors configured in a differential mode;
>
> means for providing constant current into the conductance paths of said pair of differential transistors;
>
> a second pair of transistors configured in a current mirror mode, the conductance paths of said current mirror transistors individually coupled to the conductance paths of said differential mode transistors;
>
> an hysteresis stage having a conductance path

> coupled in parallel to the conductance path of one of said current mirror transistors, said hysteresis stage responsive to a conductance state of one of said differential mode transistors for enabling current through said hysteresis stage.

Claim 8 specifies that the hysteresis stage comprises a hysteresis mirror transistor having a conductance path in series with the conductance path of a switching transistor. But claim 8 does not require that the conductance paths of the current mirror transistors be individually coupled to the conductance paths of the differential mode transistors.

Opinion

We do not sustain the rejection of claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by Sakai.

In Sakai's Figure 5, the examiner correctly identified (Paper No. 9, pages 2-3): (1) transistors Q3 and Q4 as a pair of transistors arranged in differential mode, (2) current source I_s as a means for providing constant current into the conductance paths of the pair of differential transistors, and (3) transistors Q6 and Q9 as the current mirror transistors whose conductance paths are individually coupled to the conductance paths of Q3 and Q4. These finding have not been challenged.

But the examiner has incorrectly identified (Paper No. 9, page 3) transistor Q5 as a hysteresis stage satisfying claims 1

and 8. In that regard, both claims 1 and 8 require a hysteresis stage having a "conductance path coupled in parallel to the conductance path of one of said current mirror transistors." In item D on page 3 of the final Office action (Paper No. 9), the examiner found that Sakai discloses transistor Q5 which constitutes "a hysteresis stage providing a parallel conductance path." It appears that the examiner has ignored, omitted, or not accounted for that claim language concerning the conductance path of the hysteresis stage, i.e., that it be "coupled in parallel to the conductance path of one of said current mirror transistors."

In applying Sakai, the examiner specifically referred to and relied on the Figure 5 embodiment of Sakai as the basis of his findings and analysis (Paper No. 9, page 2). Accordingly, our discussion of Sakai is also directed to its Figure 5 embodiment.

Even assuming that the examiner has found that the conductance path of transistor Q5 is coupled in parallel to the conductance path of one of the current mirror transistors Q6 and Q9, the finding is incorrect. With respect to Sakai, we do not find that the conductance path of transistor Q5 is coupled in parallel to the conductance path of either current mirror transistor Q6 or Q9.

The term "conductance path" is not explicitly defined in the

appellant's specification. However, we understand it to mean the primary current path through the device. That is consistent with the specification's description of the connection between current mirror transistors 22 and 24 and differential mode transistors 22 and 24. On page 4 of the appellant's specification, it is described that the conductance paths of current mirror transistors 26 and 28 are "series-connected" with the conductance paths of transistors 22 and 24, respectively. As is shown in the appellant's sole Figure, the drain of transistor 22 is coupled to the drain of transistor 26, and the drain of transistor 24 is coupled to the drain of transistor 28. In the case of bipolar transistors, it means "conductance path" refers to the current path between the emitter and the collector. That is also consistent with the examiner's finding (Paper No. 9, page 3) with respect to Sakai that the conductance paths of transistors Q6 and Q9 are individually coupled to the conductance paths of transistors Q3 and Q4.

In Sakai, transistor Q5's collector is coupled to neither the collector nor emitter of either transistor Q6 or Q9. Also, transistor Q5's emitter is coupled to neither the collector nor emitter of either transistor Q6 or Q9. Moreover, the base of transistor Q5 is not in direct connection with any electrode of

transistor Q6 or Q9. It cannot be said that the conductance path of transistor Q5 is coupled in parallel with the conductance path of either one of current mirror transistor Q6 or Q9.

Note that two elements being connected in parallel means the input terminals share a common node and the output terminals share a common node. That is consistent with the appellant's specification which shows transistors 34 and 36 as collectively constituting a hysteresis stage 12. There is a common node between the drain of current mirror transistor 28 and the current input to hysteresis stage 12, and a common node between the source of current mirror transistor 28 and output of hysteresis stage 12.

Further with respect to claim 8, which recites that the hysteresis stage includes a "hysteresis mirror transistor having its conductance path in series with the conductance path of a switching transistor," the examiner incorrectly found (Paper No. 9, page 3) Sakai's transistor Q5 as the switching transistor and transistor Q10 as the hysteresis mirror transistor. As can be readily seen in Sakai's Figure 5, the conductance path of transistor Q10 is not in series connection with the conductance path of transistor Q5. Rather, the collector of transistor Q10 is connected to the base of transistor Q5.

For the foregoing reasons, the rejection of claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by Sakai cannot be sustained.

Conclusion

The rejection of claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by Sakai is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
JAMESON LEE Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
RICHARD TORCZON Administrative Patent Judge	)	

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